

SECTION 3

CIRCUIT DESCRIPTIONS

3.1 INTRODUCTION

This section discusses the four major circuits that make up the Model 2150/2160. These four circuits are: measurement, motherboard, CRT, and power supply. Each of the discussions that follow, start by presenting a block diagram, then continue with a discussion of the operation of the major blocks within each diagram.

3.2 MEASUREMENT OVERVIEW

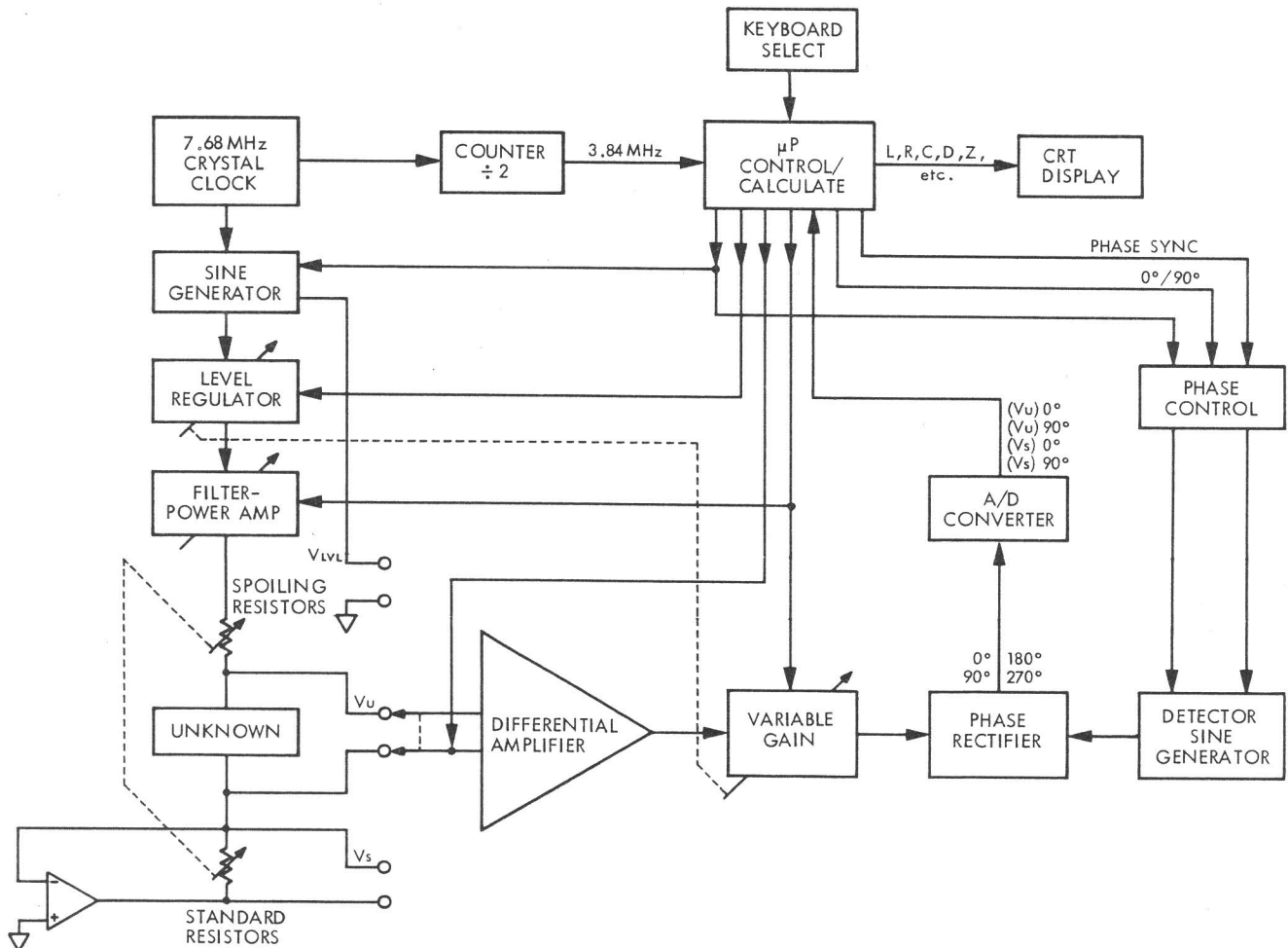


Figure 3-1. Block Diagram

The microcomputer control/calculate block is the command center for all instrument operations. It accepts input from the keyboard and coordinates all phases of a measurement sequence. It also performs all calculations required to arrive at the desired measured quantities and displays them.

Model 2150/2160 operation essentially starts with the 7.68MHz clock. This clock is divided by 2 to obtain the 3.8MHz processor clock and divided by N (1-3000) to develop the sinewave measurement signal.

The sinewave generator is frequency programmable (20Hz to 150kHz). It produces a digitally-stairstepped, sinewave output that is band limited by the filter block, then passed through the programmable level regulator. The result is a sinewave signal of specified frequency within a specified voltage range, in the mV mode, or current range, in the mA mode. This sinewave is applied to the unknown component being measured, and the standard (range) resistor.

A differential amplifier sequentially measures the voltages across the unknown component and the standard resistor. These voltages are passed through the variable gain amplifier to the phase rectifier. The phase sensitive voltmeter (phase rectifier) compares the vector relationships of the measured signals to determine which portions are in phase and which are in quadrature. The phase rectifier outputs the following four DC voltages:

V_0	or	V_{unknown}	0°
V_1	or	V_{unknown}	90°
V_2	or	V_{standard}	0°
V_3	or	V_{standard}	90°

These voltages are serially processed by the A/D converter with resistance (R) and reactance (X), or conductance (G) and susceptance (B), as computed by the Z80 CPU.

HIGH IMPEDANCE

$$G_{\text{unknown}} = \frac{V_0 V_2 + V_1 V_3}{(V_0)^2 + (V_1)^2} \times \frac{1}{R_{\text{standard}}}$$

$$B_{\text{unknown}} = \frac{V_0 V_3 - V_1 V_2}{(V_0)^2 + (V_1)^2} \times \frac{1}{R_{\text{standard}}}$$

LOW IMPEDANCE

$$R_{\text{unknown}} = \frac{V_0 V_2 + V_1 V_3}{(V_2)^2 + (V_3)^2} \times R_{\text{standard}}$$

$$X_{\text{unknown}} = \frac{V_1 V_2 - V_0 V_3}{(V_2)^2 + (V_3)^2} \times R_{\text{standard}}$$

All other impedance parameters are computed using the results of these measurements, the test frequency, and the formulas in Figure 3-2.

The calculated measurement information is displayed on the CRT screen.

SHORT CIRCUIT CORRECTION (RANGE 0)	OPEN CIRCUIT CORRECTION (RANGE 1→4)
$R_s = (R_s)_m - (R_s)_0$	$G_p = (G_p)_m - (G_p)_0$
$X_s = (X_s)_m - (X_s)_0$	$B_p = (B_p)_m - (B_p)_0$
$D = \frac{R_s}{ X_s }$	$D = \frac{G_p}{ B_p }$
$Q = \frac{ X_s }{R_s}$	$Q = \frac{ B_p }{G_p}$
$L_s = \frac{X_s}{2\pi f}$	$L_s = \frac{-B_p}{2\pi f(G_p^2 + B_p^2)}$
$L_p = \frac{R_s^2 + X_s^2}{2\pi f X_s}$	$L_p = \frac{-1}{2\pi f B_p}$
$C_s = \frac{-1}{2\pi f X_s}$	$C_s = \frac{G_p^2 + B_p^2}{2\pi f B_p}$
$C_p = \frac{-X_s}{2\pi f(R_s^2 + X_s^2)}$	$C_p = \frac{B_p}{2\pi f}$
$B_p = \frac{-X_s}{R_s^2 + X_s^2}$	$X_s = \frac{-B_p}{G_p^2 + B_p^2}$
$G_p = \frac{R_s}{R_s^2 + X_s^2}$	$R_s = \frac{G_p}{G_p^2 + B_p^2}$
$ Z = \sqrt{R_s^2 + X_s^2}$	$ Z = \frac{1}{\sqrt{G_p^2 + B_p^2}}$
$ Y = \frac{1}{\sqrt{R_s^2 + X_s^2}}$	$ Y = \sqrt{G_p^2 + B_p^2}$
$R_p = \frac{R_s^2 + X_s^2}{R_s}$	$R_p = \frac{1}{G_p}$
$X_p = \frac{R_s^2 + X_s^2}{-X_s}$	$X_p = \frac{1}{B_p}$
$G_s = \frac{1}{R_s}$	$G_s = \frac{G_p^2 + B_p^2}{G_p}$
$B_s = \frac{1}{X_s}$	$B_s = \frac{G_p^2 + B_p^2}{-B_p}$

R = Resistance
 s = Series measurement
 m = Measured value
 0 = Zero correction value
 G = Conductance

p = Parallel measurement
 X = Reactance
 B = Susceptance
 D = Dissipation factor
 Q = Quality factor

L = Inductance
 f = Frequency
 C = Capacitance
 Z = Impedance
 Y = Admittance

Figure 3-2. Model 2150/2160 Impedance Formulas

3.3 MEASUREMENT CIRCUITRY

The electronics involved with the actual measuring of a component is contained on two circuit cards. The Digital circuit card performs two basic functions: sinewave generation, and analog-to-digital conversion. The Analog circuit card holds all other measurement circuitry, i.e. level regulator, standard (range) resistors, amplifiers, phase rectifier, etc., needed to make a measurement.

3.3.1 Digital Circuit Card (P/N 53522)

3.3.1.1 Sine Generator

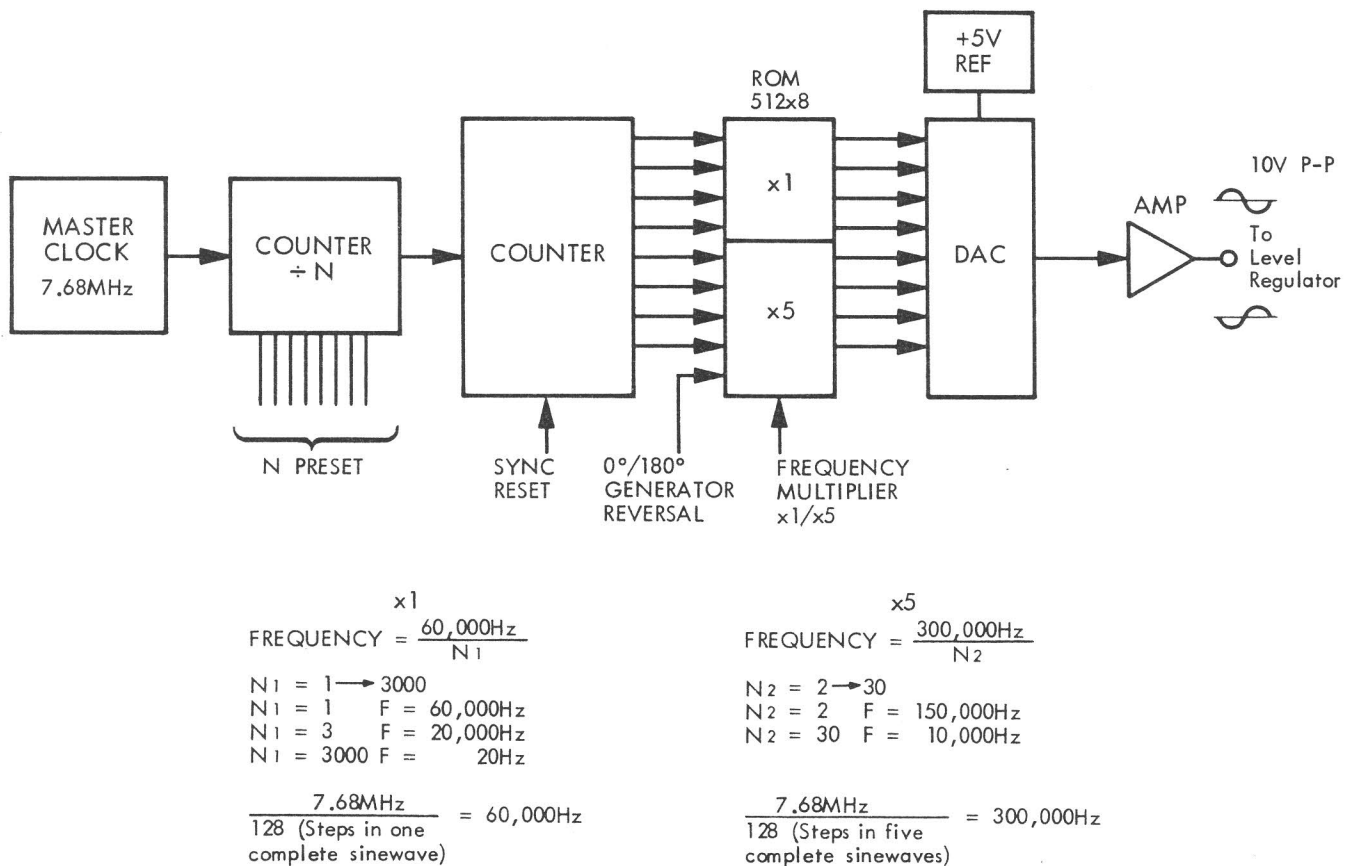


Figure 3-3. Sine Generator Block Diagram

Measurement begins when a sinewave signal at a specified frequency is applied to the unknown component. The origin of this sinewave signal is the sine generator (Figure 3-3) which consists of a preset counter chain, a second counter, a 512 x 8 bit preprogrammed ROM, a digital-to-analog converter (DAC), and a current-to-voltage buffer amplifier. The preset counter chain (U22, U24, U25) is a set of three chips configured to perform a divide-by-N function. It divides the 7.68MHz master clock into one of the 3023 frequencies that are presettable by the microcomputer. The new frequency, actually a squarewave signal, goes into a second counter chain made of U16 and U19. The second counter is connected to U17, a read only memory (ROM), in such a way that as the counter's output lines toggle, they ripple through all the addresses on the ROM. For each address the ROM outputs 8 bits of information which are fed to the D/A converter.

Twelve complete sinewave signals are stored in the 74S472 ROM in two separate locations of 256 address locations each. These locations are referred to as the X5 block (ten sinewave signals) and the X1 block (two sinewave signals, see Figure 3-3).

For test frequencies above 10kHz which divide 60,000 evenly, and for all frequencies at or below 10kHz, the X1 memory block reserves 128 address locations for the 0° sinewave and 128 locations for the 180° sinewave. Each address location contains 8 bits of information.

NOTE: 7.68MHz divided by 128 sinewave steps equals the 60kHz base frequency used to determine these test frequencies.

$$\frac{60\text{kHz}}{N} = \text{Test Frequency}$$

Where: N = 1 to 3000

For all test frequencies above 10kHz which do not divide 60,000 evenly, the X5 memory block provides an average of 128/5 or 25.6 steps for five 0° sinewaves and an average of 25.6 steps for five 180° sinewaves. This enables the ROM to store five times as many cycles (though each with fewer steps) as the X1 location.

NOTE: 7.68MHz divided by 25.6 sinewave steps equals the 300kHz base frequency used to determine these test frequencies.

$$\frac{300\text{kHz}}{N} = \text{Test Frequency}$$

Where: N = 2 to 29 (except 5, 10, 15, 20, 25)

For a complete listing of test frequencies, see Section 2.5.1.

Notice in Figure 3-3 that the counter and the ROM each have an input line coming from outside the sine generator electronics. The 0°/180° line to the ROM, under microcomputer control, selects the polarity of the ROM's output sinewave, 0° or 180°. This is the generator reversal routine where the sinewave polarity is reversed for a second series of measurements. The two series of measurements, made with opposite polarities, are algebraically subtracted to cancel offset voltages and synchronized line related pick-up.

At frequencies below 200Hz, the sync reset line to the counter is used to synchronize the 2150/2160 sinewave to the power line. The 2150/2160 detects power line zero crossings and starts its sinewave at these exact points. This is accomplished by resetting the counter at the first power line zero crossing after a completed measurement cycle. Test signal/power line synchronization maximizes rejection of line related electromagnetic interference (EMI) in the measurement circuit.

At frequencies above 200Hz, the EMI level decreases so that line synchronization is not necessary. Neither linelock time nor the additional settling time provided by generator reversal is required. U12 provides a detector reversal technique which also cancels op amp offsets, but settling time only occurs once at the beginning of the measurement sequence. This results in faster measurement speeds above 200Hz.

The digital-to-analog converter (DAC) is the analog device that produces the actual waveform. It works with operational amplifier U14 to transform the DAC's current output into a voltage waveform. The sine-wave output from the sine generator is 10V peak-to-peak and is symmetrical around zero.

3.3.1.2 Analog-to-Digital Converter

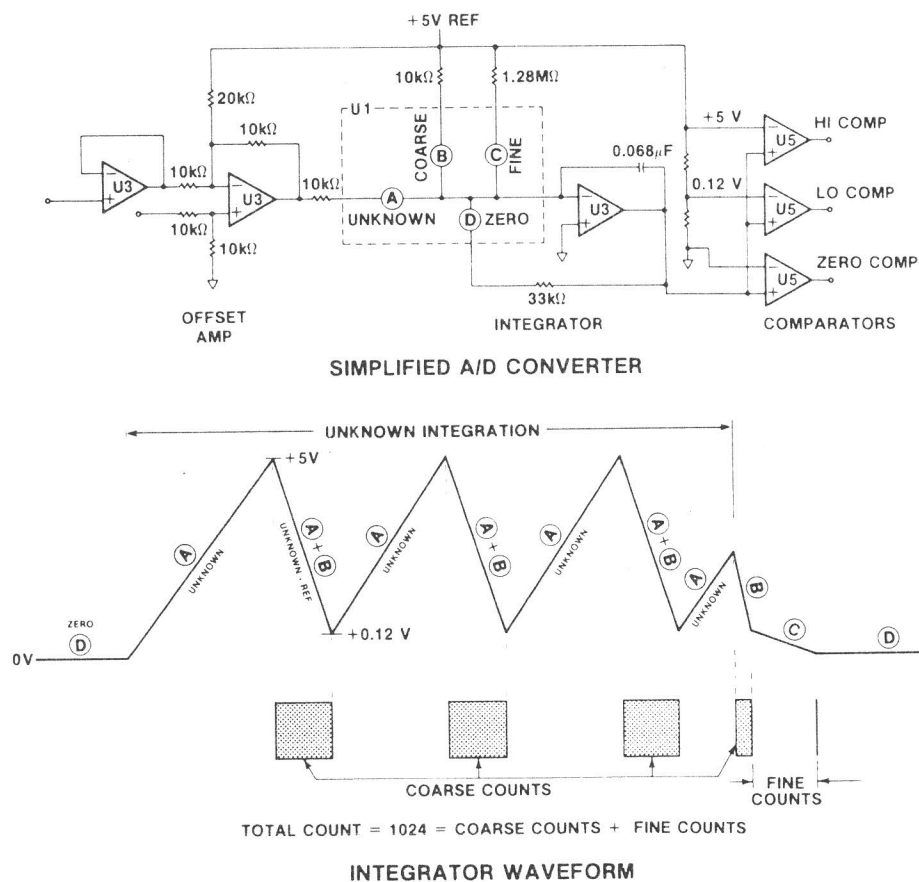


Figure 3-4. A/D Converter Simplified Diagram

The analog-to-digital converter is called a "charge balancing" A/D converter (see Figure 3-4). Moving from left to right on the diagram, the offset amplifier, two sections of quad-amplifier U3, offsets the DC input voltages, from the phase rectifier, so they always remain one polarity. Solid state switch, U1, selects inputs, i.e. unknown signal, standard signal, coarse reference, fine reference, or zero, to the third section of U3, the integrator. Three comparator sections of U5, and logic U7, U8, U6, and U11 (see schematic diagram in Section 5 of this manual), synchronize the turning ON and OFF of coarse and fine counters with the switching of coarse and fine reference inputs to the integrator. Counter timer, U29, has 3 channels: two channels are counters, one for coarse counts, and one for fine counts during A/D conversion, and the third channel sets up, through the bus system, the number of multiples of test frequency over which the integrator will integrate. The 2150/2160 is locked into exact multiples of the test cycle or test frequency because it is the test frequency that determines the actual integration time. The Digital assembly also contains support logic for the A/D converter. The support logic interfaces the A/D converter's output to the microcomputer, and performs level shifting for the drive signals to the input (reference) switches on the integrator. The easiest way to step through the A/D conversion sequence is to follow the integrator waveform (in Figure 3-4). The circled letters on the waveform correspond to the input (reference) switches in the simplified diagram.

The integrator waveform starts from the 0V level. When switch A is turned ON, the integrator starts ramping toward the +5V level. (Switch A allows the unknown signal, a DC voltage from the phase rectifier, to pass to the integrator.) Upon reaching the +5V level a comparator, called "HI COMP", causes the logic to turn switch B, the coarse reference, ON. With both switches ON, the integrator ramps back down toward zero. It ramps down to approximately +0.12V where the "LO COMP" comparator trips turning the B switch OFF. With the A switch ON by itself again, the integrator ramps back up toward +5V. Switch B comes back ON at the +5V level, and the integrator ramps down toward zero. The object of this switching technique is to keep the integrator in bounds, between +5V and +0.12V, for the duration of the unknown integration. This allows longer integration times without the integrator going out of range and provides a wide choice of integration times and also provides shorter total integration time due to the overlap of the reference signal with the unknown integration.

At the end of the unknown integration, switch A is turned OFF. (It remained ON during the unknown integration.) Now, since the integrator is still above the 0V level, switch B is turned ON driving the integrator to the 0.12V level, then is turned OFF and switch C is turned ON. Switch C is called "fine" reference. The fine reference brings the integrator back to 0V.

The relationship between coarse and fine reference levels lies in the fact that they each have an associated counter. Each time the B switch is turned ON, a counter is being gated to keep track, by accumulating counts, of how long switch B was on. (In Figure 3-4, the waveform has four bursts of coarse counts, three of which are roughly the same level, the fourth is a finish off of the coarse counts.) The fine counter also accumulates counts when switch C is turned ON. The relationship, for counts, is one coarse count equals 1,024 fine counts.

Where does this 1,024 count relationship come from?

Looking carefully at the coarse and fine reference levels, you find that the coarse and fine differ by a factor of 128, not by 1,024. The clocks associated with the coarse counter and the fine counter are not the same, one clock is 120kHz, that is the coarse count clock, and the fine clock is 8 times that or 960kHz. As a result there is a factor-of-8 difference, and 8 times 128 equals 1,024.

The total of all coarse and fine counts constitutes a measured value. Accumulated counts for each of the four measured values ($V_{\text{unknown } 0^\circ}$, $V_{\text{unknown } 90^\circ}$, $V_{\text{standard } 0^\circ}$, $V_{\text{standard } 90^\circ}$) are sent to the micro-computer.

3.3.2 Analog Circuit Card (P/N 53675)

3.3.2.1 Signal to the Unknown

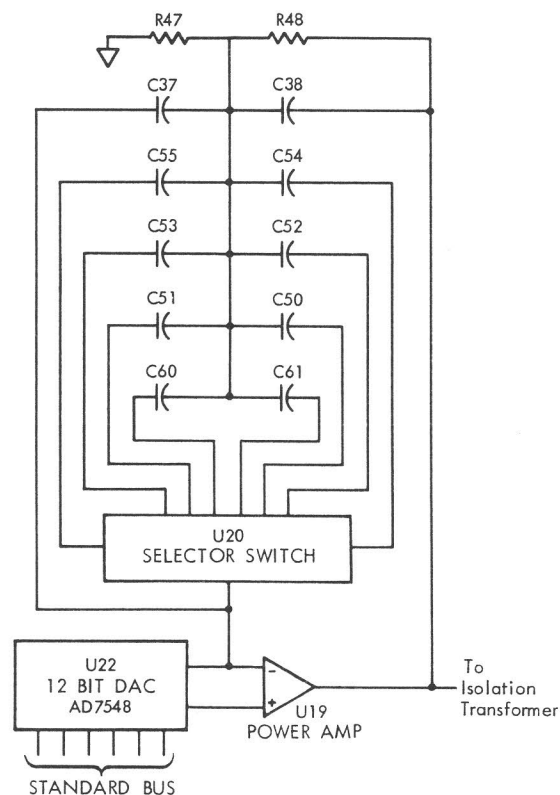


Figure 3-5. Level Set, Filter, and Power Amplifier Block Diagram

As the sinewave from the sine generator comes onto the Analog circuit card, it goes through a level-setting DAC. The level-set DAC is a twelve-bit converter under microcomputer control. It can reduce the test signal to any one of 4096 predetermined test levels. This level-set DAC, U22, is ganged with U17, the variable gain DAC. Then, as the test signal level is reduced, the measured signal can be amplified by the same amount for further processing.

The level-set DAC outputs a stairstepped sinewave that must be filtered before it can be used. The Analog assembly has five filters that can be selected for this job. Filter selection is dependent on the test signal frequency:

- C60 and C61 are selected at frequencies below 200Hz,
- C50 and C51 between 200Hz and 2kHz,
- C52 and C53 between 2kHz and 20kHz,
- C54 and C55 between 20kHz and 42.8kHz,
- C37 and C38 between 42.8kHz and 150kHz.

The filtered sinewave is sent to the power amplifier.

The power amplifier consists principally of op amp U19 and transistor array Q2. The output of Q2 supplies enough current through the HI DRIVE port to the unknown so a measurement can be made. The power amplifier also supplies a signal to the isolation transformer and the high side of the standard (range) resistors.

3.3.2.2 Range Switching

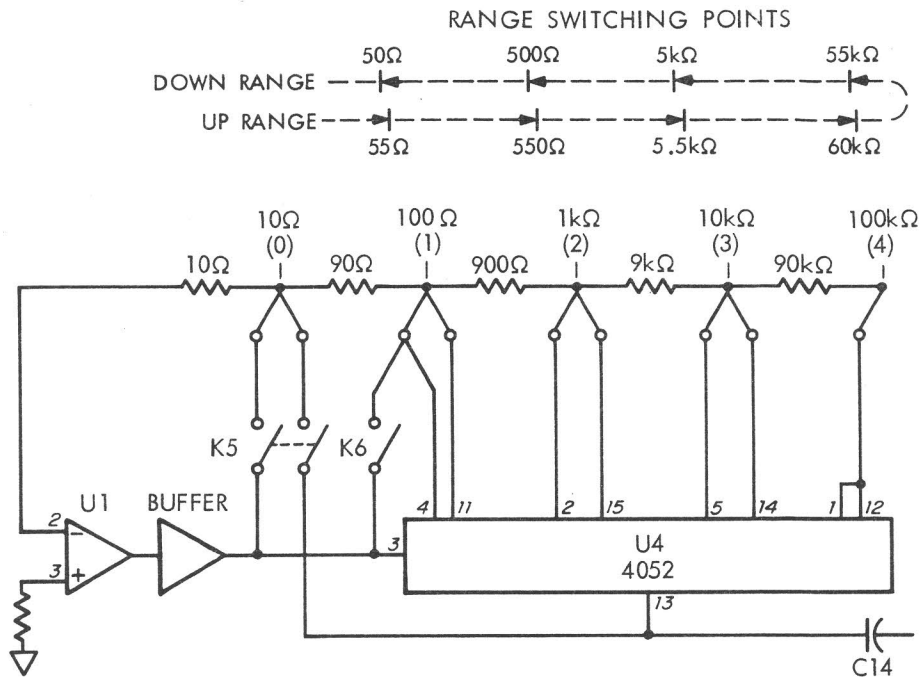


Figure 3-6. Range Switching Block Diagram

Figure 3-6 illustrates the range switching used in the 2150/2160. The diagram shows the standard resistor combinations used to configure any of the resistance ranges, 0 through 4. Due to higher current present at the low impedance ranges (0 and 1), relays K5 and K6 are used to switch the 10Ω and 90Ω standard resistors in/out of the feedback circuit, while the 900Ω, 9kΩ, and 90kΩ resistors are switched by solid state switch U4. The op amp, U1 and buffer force all current to pass through the selected range resistor. Voltage sensing is provided by the extra contact point at each range value.

Range 4 (100kΩ) is locked out above 10kHz due to stray capacitance effects.

3.3.2.3 Series Spoiling Resistors

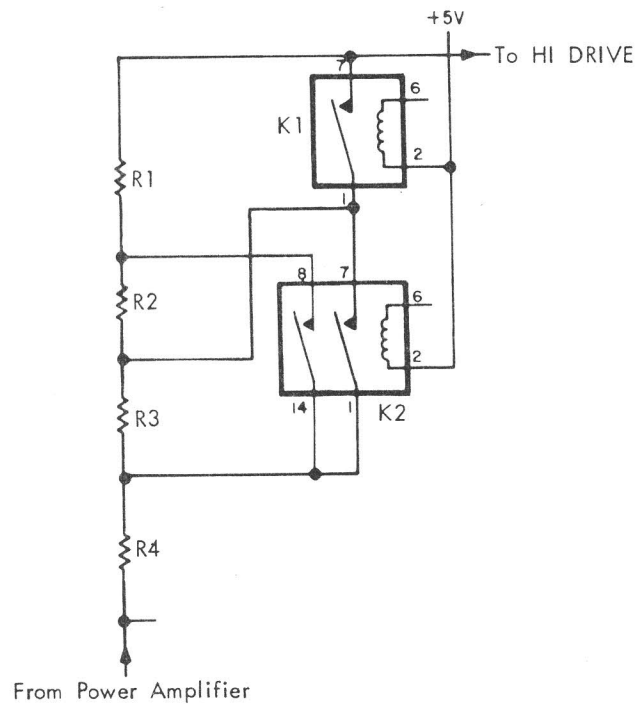


Figure 3-7. Series Spoiling Resistors

Series spoiling resistors, R1 thru R4, stabilize the instrument for reactive unknowns. Each resistor is placed in series with the unknown by relays K1 and K2. The spoiling resistors are changed in conjunction with a corresponding standard resistor.

3.3.2.4 Phase Trims

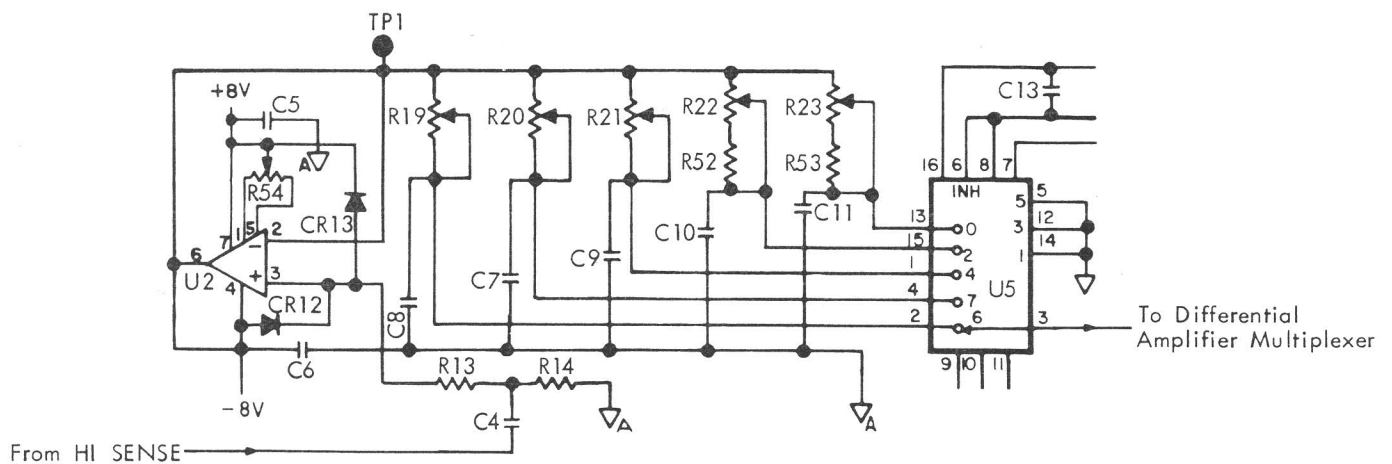


Figure 3-8. Phase Trims

Phase calibration trimmers R19 thru R23 and R40 calibrate dissipation factor for each measurement range. They compensate for phase differences between the unknown and standard measurement channels. Solid state switch U5 changes the phase trim when the corresponding range resistor is changed.

3.3.2.5 Differential Amplifier

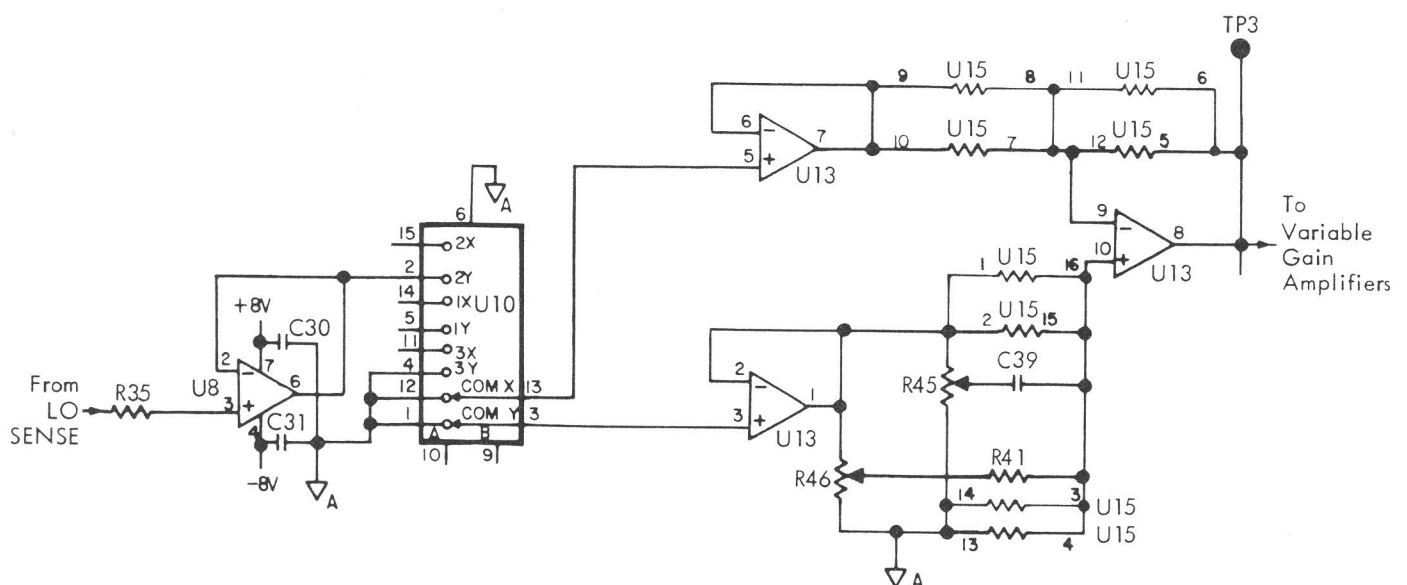


Figure 3-9. Differential Amplifier

The differential amplifier consists of 3 sections of quad-amplifier U13. Its input is sequentially selected by the input multiplexer U10. The multiplexer selects either the voltage drop across the unknown, the voltage drop across the standard (range) resistor, or the 1.0V RMS reference voltage for measurement. The reference voltage is measured first. The measured reference voltage is recorded as a reference number of counts (A/D converter counts) against which the measured unknown and standard signals are compared.

3.3.2.6 Variable Gain Amplifier

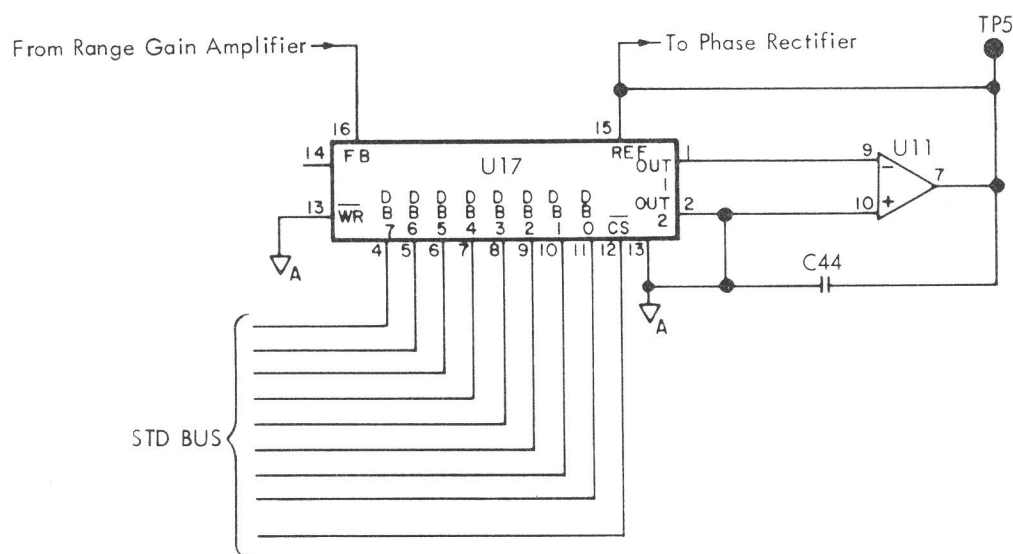


Figure 3-10. Variable Gain Amplifier

The variable gain amplifier (VGA), U17, works in conjunction with the level set and the range gain to boost the measured signal to the proper operating levels for the phase rectifier. The VGA is a programmable DAC capable of producing signal gains of 1 to 256.

3.3.2.7 Overload Detector

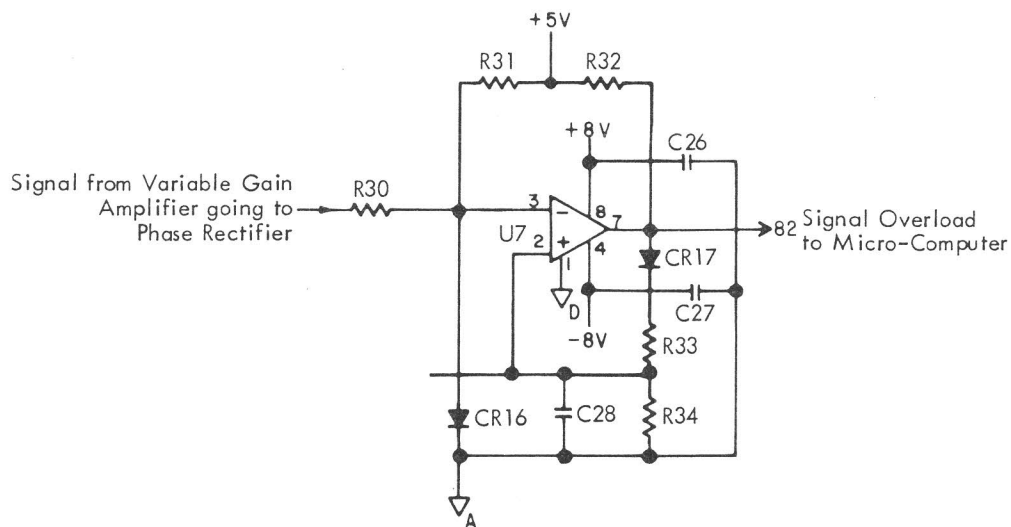


Figure 3-11. Overload Detector

Overload detector U7 monitors the signal going from the output of the variable gain amplifier to the phase rectifier. This peak detector indicates overload when the signal is too high. The detector's output goes HI when an overload occurs and the VideoBridge display results in an error message of "ERROR Analog".

See Section 2.11 for error message descriptions.

3.3.2.8 Phase Rectifier

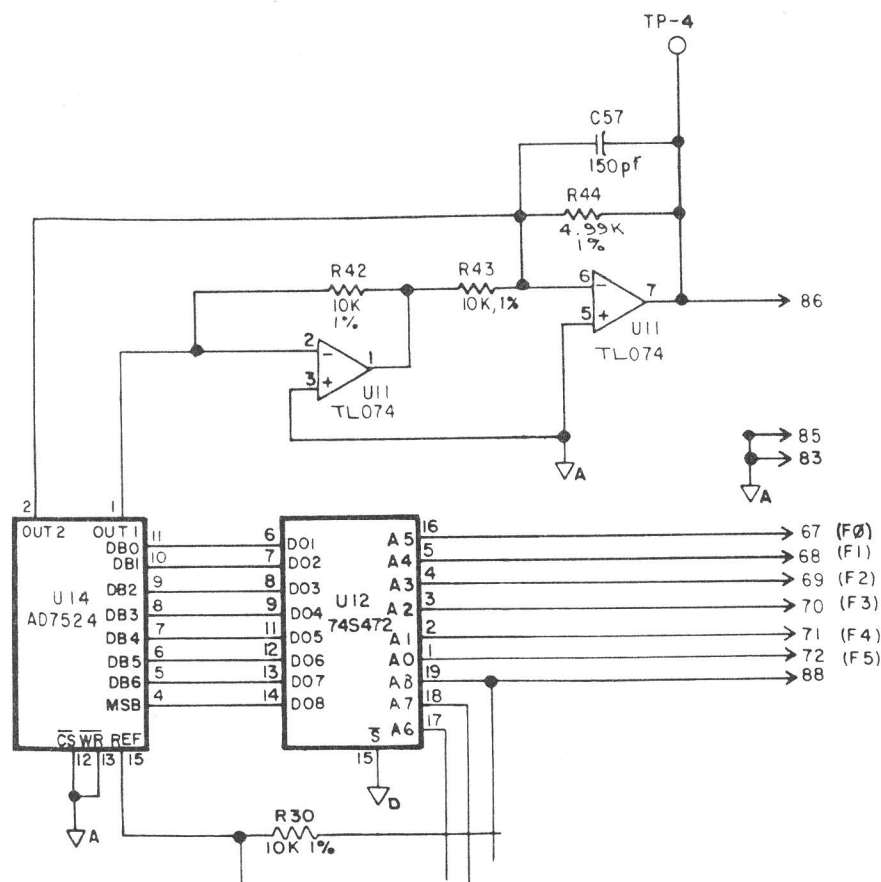


Figure 3-12. Phase Rectifier

The phase rectifier, shown in the Block Diagram, resides in U14, U12, and U11; a four quadrant, CMOS digital-to-analog converter. The phase rectifier is driven by a 512 x 8 bit PROM which does the synchronous gating needed to give a DC output. The PROM is driven by six input lines that are harmonics of the test frequency. Three other input lines are used to select the 0°/90° bit, 0°/180° bit, and LOW/HIGH frequency bit. This circuit provides a multiplier type action of phase detection. It takes the product of the sinewave (measured signal) coming in and the digitally related sinewave (from the PROM) to produce a DC current output. The current output of U14 is summed by two sections of operational amplifier U11 to produce a full wave voltage output.

3.4 MOTHERBOARD

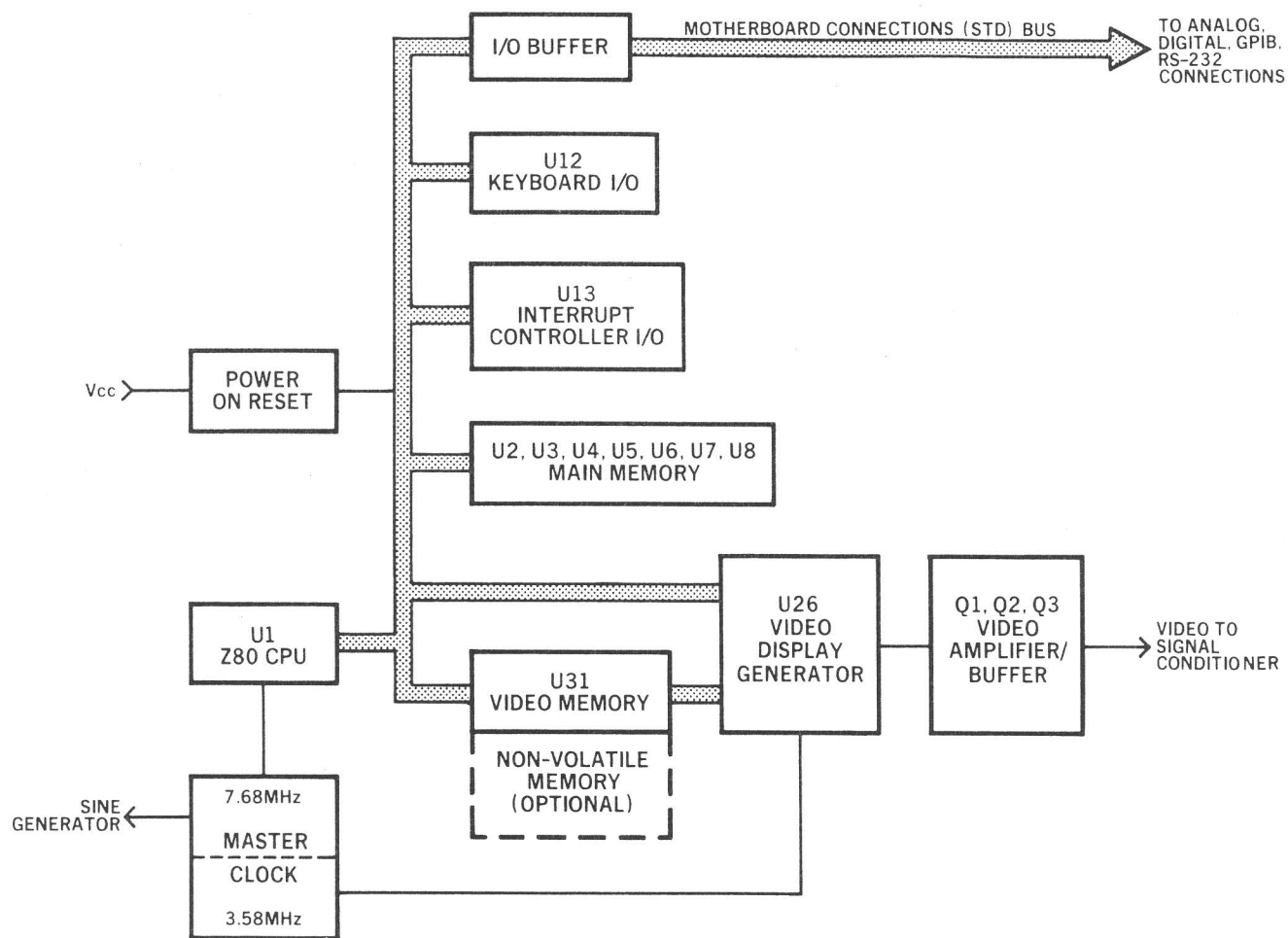


Figure 3-13. Motherboard Simplified Diagram

A simplified diagram of the motherboard is shown in Figure 3-13. The motherboard architecture centers on its standard communication bus which has 6 slots for plugging in circuit cards containing measurement circuitry, IEEE-488 interfacing circuitry, RS-232C interfacing circuitry, and other bus compatible devices. The motherboard holds the Z80 CPU chip and its memory, the video generator and its memory, the master clock, and associated control logic.

3.4.1 CPU

The central processing unit (CPU) used in the 2150/2160 is a Z80 microprocessor chip. It has complete control of all functions of the instrument and does all the calculations required to arrive at the desired measured quantity. The CPU, when joined with the keyboard I/O (U12), interrupt controller I/O (U13), and main memory PROM, ROM, or RAM (U2 thru U8), comprise the 2150/2160's internal microcomputer.

A computer bus exists to convey information from the CPU to its peripherals. To do this the CPU must supply, and the bus must convey certain specific information such as:

1. What information?
2. To whom? To what destination?
3. When is the information valid?
4. When is the destination name valid?

The exact information is conveyed over an 8 bit DATA bus, the source or destination of the information is conveyed over a 16 bit ADDRESS bus, and the "whens" are resolved by CONTROL lines. The DATA bus, ADDRESS bus, and CONTROL lines are combined into one set of parallel lines, on the motherboard, called the standard (STD) bus.

Any CPU can support only so many capacitive, and only so many DC loads. Expansion beyond these load limits requires buffering. All ADDRESS, DATA, and CONTROL lines are buffered before they are routed to the standard (STD) bus. Thus, all devices that talk to the CPU can be divided into two groups: those that exist on one side of the buffers (that talk directly to the CPU), and those that exist on the other side of the buffers (that talk to the CPU through the buffers). It is the job of the motherboard's logic to decide on which side of the buffers a device is and whether or not to enable those buffers. If an addressed device is on the CPU side of the buffers (INTERNAL), it needs to be singled out (SELECTED) before it can speak or be spoken to. Devices that are INTERNAL are:

1. Keyboard I/O, KD118279, U12
2. Interrupt controller I/O, CTC3882, U13
3. Video display generator control, MC6847, U26
4. Video memory, RAM, U31
5. Main memory, PROM, ROM, or RAM

Logic on the motherboard is programmed to know the addresses of these INTERNAL devices. For all devices not INTERNAL, the motherboard logic presumes that they reside somewhere off the motherboard, and the appropriate buffers are enabled.

I/O decode is accomplished with two MSI (Medium Scale Integration) address comparators, U11 and U9. U11 is a comparator which is set to recognize a range of I/O addresses. This range is subdivided by the 74LS139 which is a 2:4 line decoder/selector. When U11 recognizes a valid INTERNAL I/O address it selects the decoder which resolves the address, allowing one particular INTERNAL I/O device to communicate with the CPU.

Memory decode is accomplished with U14, which is a 32 x 8 bit fused link ROM. The inputs to the ROM are address lines, the ROM is programmed to do a table lookup: "this address in, means this chip select out." The chip-select outputs are routed to one of the INTERNAL memory sockets (U2 thru U8). Note that U14 is doing the same job for the memory as the comparator and selector are for the I/O.

Also note that these are more than just address lines entering the comparator chips in both of the previous circuits, these are the CONTROL lines that tell the comparator when the address is valid and when a chip select can be output.

3.4.2 Standard Communications Bus

When the CPU addresses a device on the output side (EXTERNAL) of the CPU buffers, it also needs to be singled out (SELECTED) before it can speak or be spoken to. There are a number of lines, called the standard (STD) bus, that are dedicated to conveying address information, control signals, and data to and from these EXTERNAL devices. The STD bus has six locations for plugging in measurement and I/O dedicated devices. Standard bus signals and card edge connections are identified in Table 3-1. Devices that are serviced by the STD bus are:

1. Digital and Analog Measurement circuit assemblies.
2. GPIB circuit assembly (optional).
3. RS232 Interface circuit assembly (optional on 2150).
4. Cassette tape interface (Model 2160 only).

Table 3-1. Standard Bus Signals and Card Edge Connections

	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5 V	In	+5 Volts DC (Bussed)	2	+5 V	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5	-5 V	In	-5 Volts DC	6	-5 V	In	-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP*	In/Out	I/O Expansion	36	MEMEX*	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	NA	CPU Machine Cycle Sync
	39	STATUS 1*	Out	CPU Status (Z80-M1)	40	SATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock Processor 4.0MHz	50	CNTRL*	In	CPU Clock 3.84MHz
	51	PCO*	Out	Priority Chain Out	52	PCI*	In	Priority Chain In
POWER BUS	53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
	55	AUX + V	In	AUX Positive (+12 Volts DC)	56	AUX - V	In	AUX Negative (-12 Volts DC)

*Low Level Active Indicator

3.4.3 Extra Bus

Some EXTERNAL devices used in the 2150/2160 communicate with signals that are not compatible with the STD bus. For these devices, a second proprietary bus called the extra bus is used. The extra bus is designed to carry analog signals as well as digital information. The extra bus transmits the following major signal categories (see Table 3-2 for a further breakdown of signals):

1. 7.68MHz clock signal
2. Sinewave test signals
3. Chip select signals
4. Measurement cycle and zero crossing information
5. Remote start

Table 3-2. Extra Bus Signals and Card Edge Connections

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
57	AUX GND	AUX Ground (Bussed)	58	AUX GND	AUX Ground (Bussed)
59	AUX +V	AUX Positive (+12VDC)	60	AUX -V	AUX Negative (-12VDC)
61	IO1	I/O Select	62	IO2	I/O Select
63	IO3	I/O Select	64	IO4	I/O Select
65	60Hz	60Hz Square Wave	66	7.68MHz	128 x 60 kHz
67	F0	Test Frequency Square Wave	68	F1	2 x F0 (F0→F6 connect to sine ROM Address Pins)
69	F2	4 x F0 (F0→F6 connect to sine ROM Address Pins)	70	F3	8 x F0
71	F4	16 x F0	72	F5	32 x F0
73	F6	64 x F0	74	FINE GATE	Analog Gate Control
75	HI GATE	Analog Gate Control	76	LO GATE	Analog Gate Control
77	Z GATE	Analog Gate Control	78	JNK	Analog Gate Control
79	HI CMP	Comparator Control	80	LO CMP	Comparator Control
81	Z CMP	Comparator Control	82	SIG OVERLOAD	Comparator Control
83	SINE GND	Ground	84	SINEWAVE	Buffered Sinewave
85	LO-V _{IN}	A/D Converter Control	86	HI-V _{IN}	A/D Converter Control
87			88		
89			90		
91			92		
93			94		
95	CPU BUSY	Indicates Internal Process	96	START	Start Measurement
97	-7.5V	500mA CMOS Switches	98	+7.5V	500mA CMOS Switches
99	GND	Ground	100	GND	Ground

3.4.4 Clock Signals

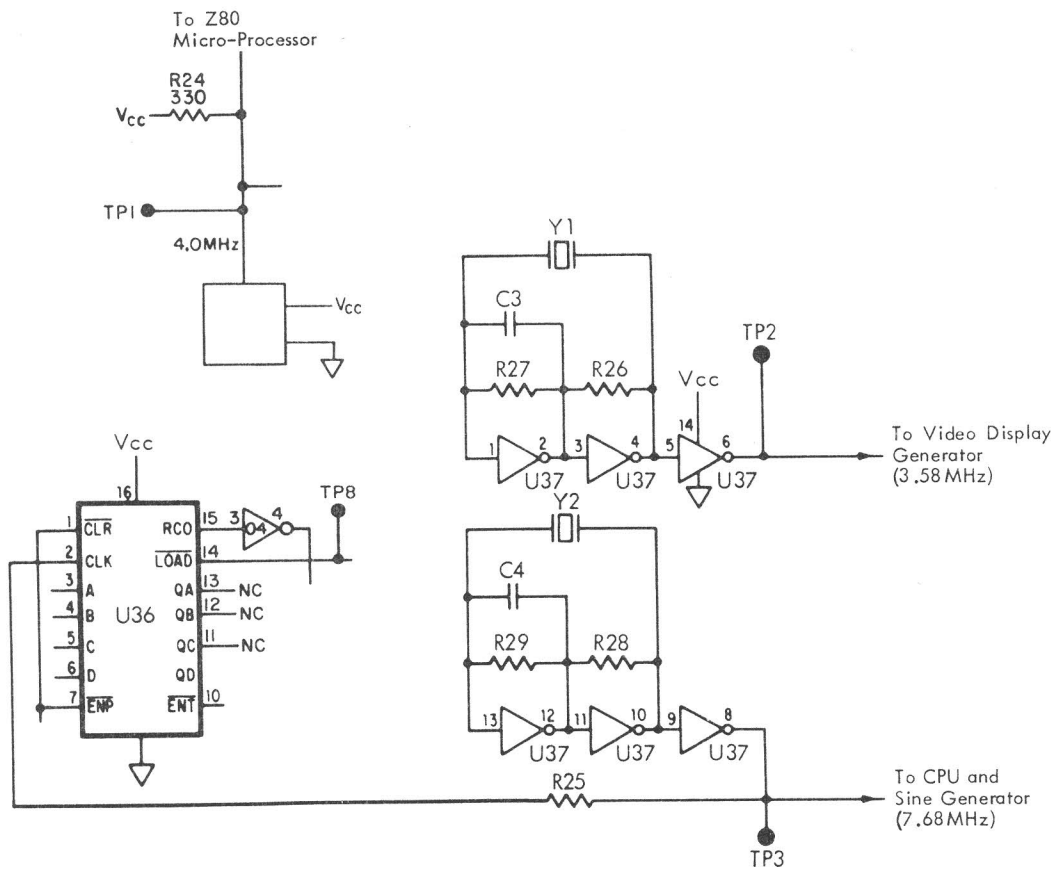


Figure 3-14. Clock Signals

Three clock oscillators are located on the motherboard. One clock signal of 4.0MHz is sent to the CPU to set processor speed. It can be monitored at TP1.

A second clock signal is a "color burst" frequency (3.58MHz) produced by Y1 and used for the video display generator. It can be monitored at TP2.

The third clock signal of 7.68MHz is produced by Y2 and divided by 128 to provide the 60kHz base frequency used by the sine generator. It can be monitored at TP3.

3.4.5 Power ON Reset

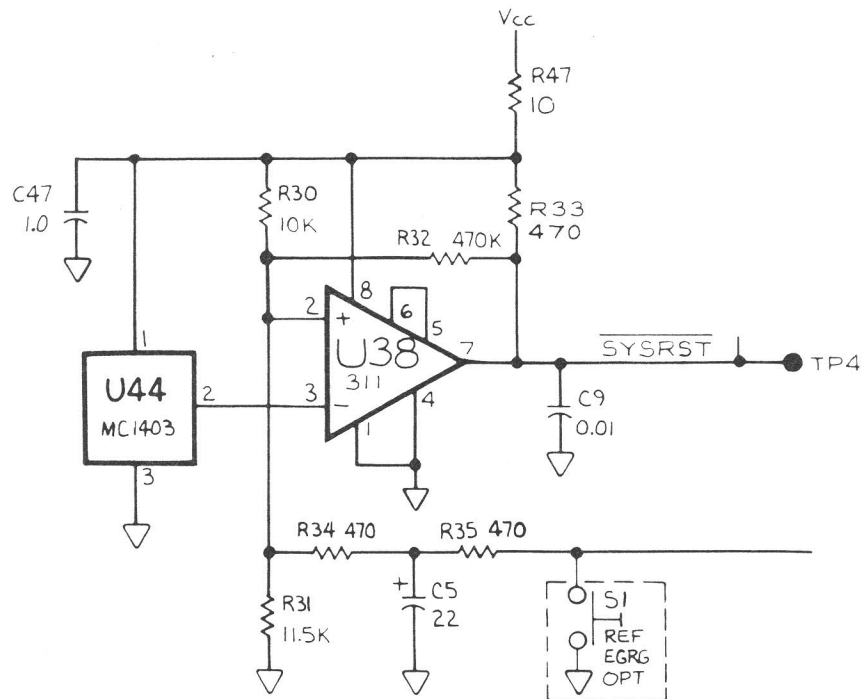


Figure 3-15. Power ON Reset

The power ON reset circuitry is necessary because of the long power-up time of the switching power supply. During power-up, the output of U38 (SYSRST) is active LO. This resets all logic circuitry and maintains this level until V_{cc} reaches 4.8 volts. Capacitor C5 then provides a slight time delay of about 1/10 second before the output of U38 is allowed to go HI and release the reset line. If V_{cc} should subsequently fall below 4.5 volts (usually due to line voltage variances), SYSRST will again go LO until V_{cc} is restored to its operating level of 4.8 volts.

3.4.6 Video Display Generator

The video display generator (VDG) is a Motorola MC6847 which accepts a binary control word gated into it from the microcomputer. In response to that binary input, the VDG creates characters, graphic, and semi-graphic information that is output in a format that corresponds to a normal television raster scan arrangement.

The VDG has memory chip U31 associated with it which stores a screen of information to be scanned and displayed. The video memory has two operating modes. Initially, the VDG has access to the memory and is always scanning and converting the memory contents to characters then sends those characters out to the video display. When the processor is ready to read or write a character into that memory, it goes through a piece of arbitration logic that says, if the video display generator is doing a horizontal sync, a horizontal retrace, or a vertical sync, then grant the processor access to the memory. However, if the VDG is not doing horizontal sync or vertical sync, then it is putting video out and must not be interrupted. At that point the processor is told to wait, treating the video memory like slow memory. The processor will wait, keeping the address, data, and control lines activated, until a horizontal sync or a vertical sync is output, then the memory returns to normal operation and readily accepts new inputs from the processor.

The composite video, as it comes out of the VDG chip, is a very low level signal. The signal is high impedance in nature and is very susceptible to noise and interference. To counteract these undesirable qualities, there is a two transistor amplifier/buffer (Q1, Q2,) that transforms the VDG output signal into a higher level, low impedance output signal. This output signal drives the video section of the 2150/2160.

3.5 VIDEO CIRCUITRY

DANGER

THE VIDEO CIRCUITRY CONTAINS DANGEROUSLY HIGH VOLTAGE. EXERCISE EXTREME CARE TO AVOID POSSIBLE ELECTRIC SHOCK WHICH MAY RESULT IN SEVERE INJURY OR DEATH.

All video display circuitry for the 2150/2160 is contained on one circuit card. It provides all the signal processing required for displaying video information on the CRT screen. Operation of the video circuitry is discussed in the following paragraphs.

Refer to Section 5, schematic diagram P/N 48642 for the following discussions.

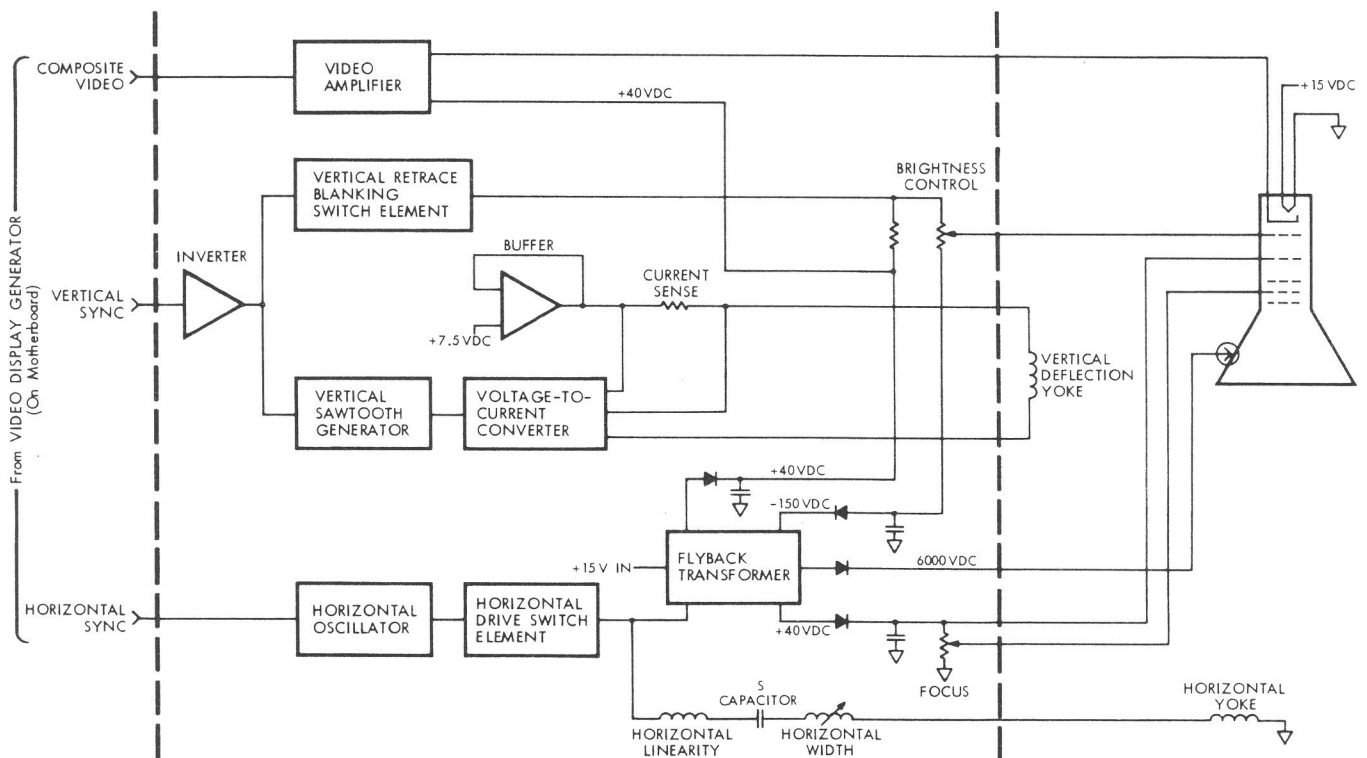


Figure 3-16. Video Circuit Block Diagram

3.5.1 Video Amplifier

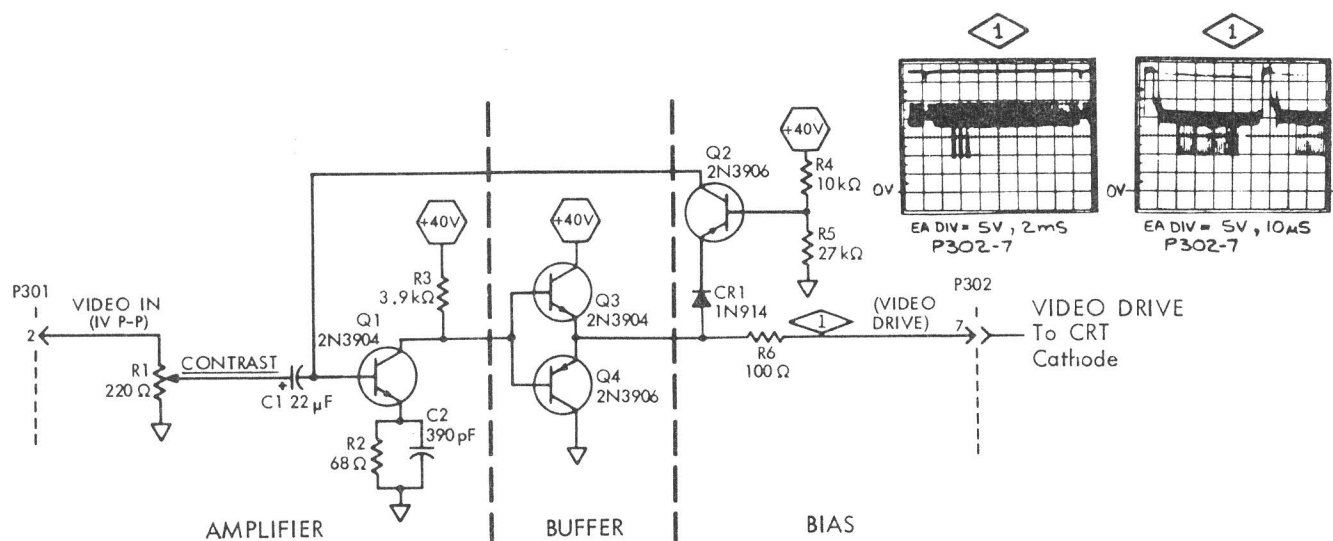


Figure 3-17. Video Amplifier

The Video Amplifier circuitry serves two purposes:

1. Amplify the composite video signal from the Video display generator.
2. Drive the CRT cathode with the necessary signal to produce the display.

The following paragraphs will discuss these two functions in detail.

The composite video input signal is applied to potentiometer R1, the contrast control. The contrast control adjusts the level of the composite video signal going to the Video Amplifier. This signal is coupled through capacitor C1 to a fixed gain amplifier consisting of Q1, R3, R2, and C2. The AC gain of the stage is fixed by R3, R2, and emitter bypass capacitor, C2. Capacitor C2 is matched against circuit board strays to maintain the bandwidth of the stage at 10MHz. Transistors Q3 and Q4 act as a buffer for amplifier Q1.

Bias for Q1 is derived from the DC restoration circuitry consisting of

3.5 VIDEO CIRCUITRY

DANGER

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All video display circuitry for the 2150/2160 is contained on one circuit card. It provides all the signal processing required for displaying video information on the CRT screen. Operation of the video circuitry is discussed in the following paragraphs.

Refer to Section 5, schematic diagram P/N 48642 for the following discussions.

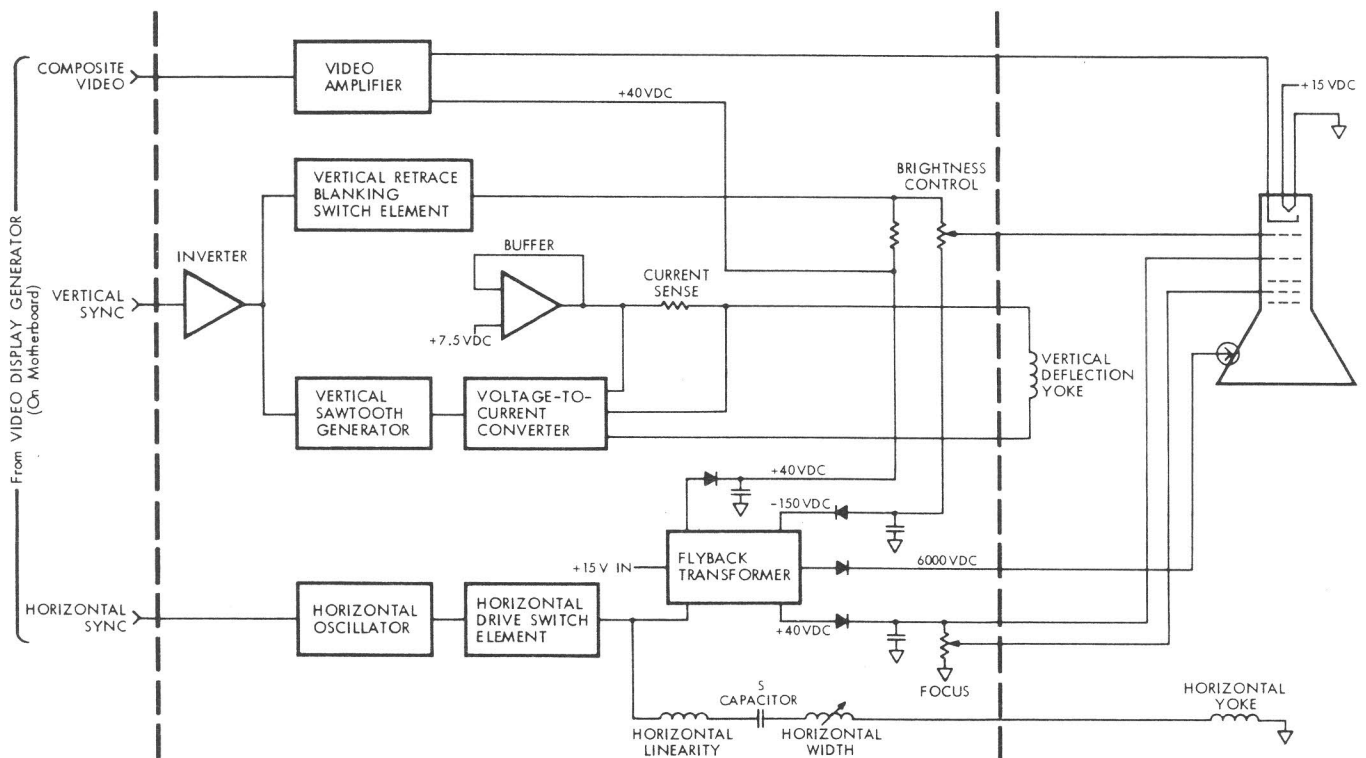


Figure 3-16. Video Circuit Block Diagram

Resistor R6 provides current limiting for Q3 and Q4 should the output at pin 7 be shorted to ground. The output of the stage can have voltage swings in the vicinity of 0VDC to 30VDC which are the levels required when composite video is applied to the cathode of the CRT. These voltage swings will turn the CRT from full-on to full-off providing crisp black and green, and some half-tone displays.

One of the requirements of a video circuit such as the one used in the 2150/2160 is blanking the electron beam whenever one frame has been completed and the electron beam is going to be retraced from the end of one frame up to the beginning of the next one.

The Vertical Sync signal is fed to inverter Q5 which in turn feeds the signal to the gate of a VFET, Q6. Transistor Q6 provides the blanking signal during the vertical retrace. When the Vertical Sync signal is in its active state as a low-going peak at P301 - Pin 4, inverter Q5 is in its off condition. With Q5 off, Q6 turns on forcing the junction of R10 and R11 to ground. With R10 and R11 at ground, the potential at the wiper of potentiometer R33 is -40VDC as set by the voltage divider of R11, R33, and R12. This -40VDC is fed to the brightness grid of the CRT, producing a black display. When the Vertical Sync signal is in its inactive state as a high level at P301 - Pin 4, Q5 is turned on forcing Q6 off. With Q6 off, the junction of R10 and R11 becomes more positive as determined by the divider string of R10, R11, R33 and R12. With the junction of R10 and R11 at a more positive potential, then the wiper of R33 becomes less negative such that the proper bias is supplied to the brightness grid producing a green display. Potentiometer R33 is available at the rear of the 2150/2160 for adjusting the brightness of the display.

Capacitor C3 provides a low impedance path for electrostatic noise which could be coupled into the brightness grid from the flyback transformer causing brightness variations.

3.5.3 Vertical Drive

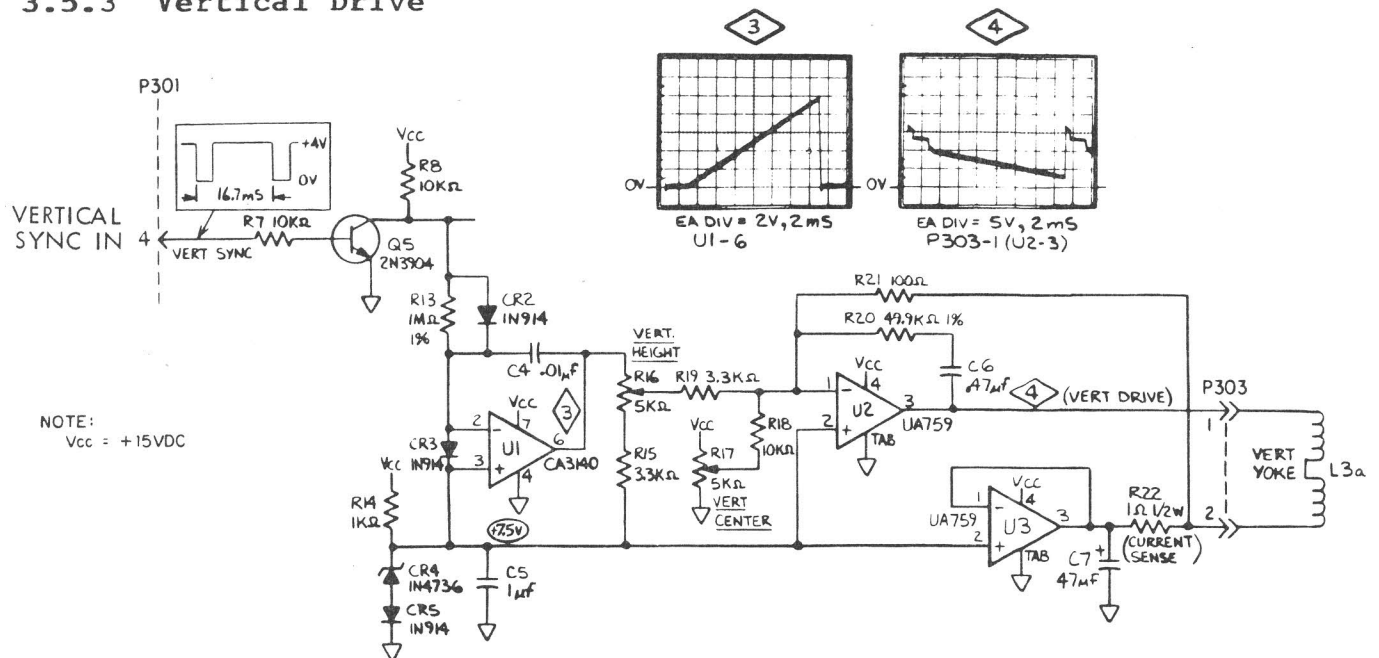


Figure 3-19. Vertical Drive

The Vertical Sync signal comes in on pin 4 of P301 and is fed to inverter Q5. Amplifier U1 is the active element for the vertical sawtooth generator. The vertical sawtooth generator transforms these vertical sync input pulses into a linear, sawtooth voltage waveform that will eventually drive the vertical deflection yoke. The sawtooth generator operates as follows:

During the positive portion of the vertical sync signal, inverter Q5 is turned on pulling its output low. This provides a near ground signal to the input resistor of U1 (R13) causing the feedback capacitor C4 to charge in a positive direction. Capacitor C4, resistor R13, and the voltage across R13 define the slope of the rising output. During the low level of the vertical sync signal, inverter Q5 is turned off with its output pulled to +15VDC by pull-up resistor R8. This provides a positive signal to the inverting input of U1 causing the feedback capacitor C4 to discharge back to zero. The discharge rate is much faster than the charge rate due to the action of diode CR2 which is forward biased during the low level of the vertical sync pulse, yielding a slope much greater than that during the positive part since R13 is bypassed during this cycle.

The voltage-to-current converter, U2, transforms the sawtooth voltage waveform at its input resistor, R19, to a sawtooth current at its output to drive the vertical yoke. Resistor R16 provides vertical height adjustment of the picture on the CRT by controlling the amplitude of the sawtooth waveform from the sawtooth generator. Resistor R17 is a DC offset adjustment for U2 which allows for adjusting the vertical centering of the picture on the CRT.

Amplifier U3 is a buffer between the common bus and sense resistor R22. Resistor R22 senses the current from the voltage-to-current converter U2. The resultant voltage drop across R22 is summed with the output from U1 and fed back to the input to U2. The action of the R22 sense feedback is referenced against a stable common bus to maintain linearity throughout the vertical sweep. Resistor R20 and capacitor C6 prevent amplifier U2 from oscillating while driving the vertical yoke.

3.5.4 Horizontal Drive

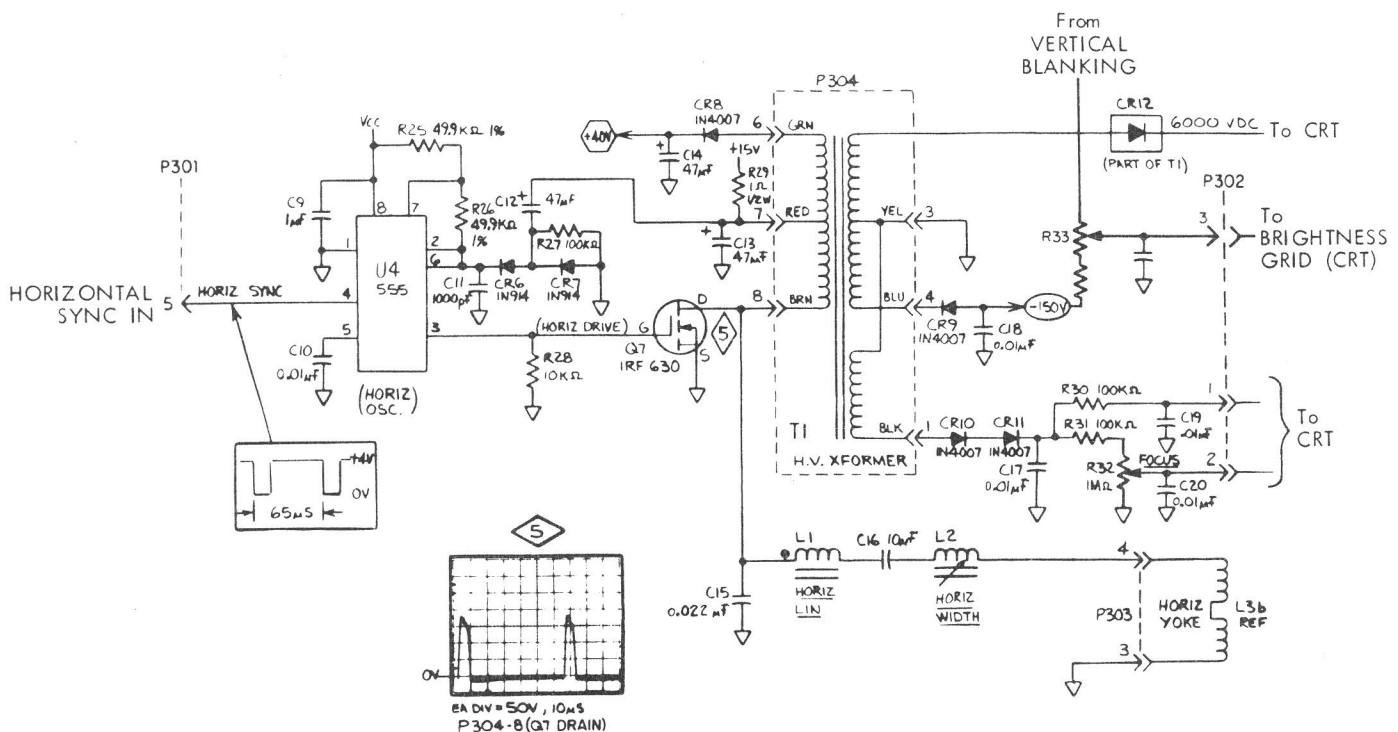


Figure 3-20. Horizontal Drive and High Voltage

3.5.4 Horizontal Drive

The Horizontal Sync signal comes in on pin 5 of P301 and is fed to the horizontal oscillator, U14. The synchronized oscillator is used to provide drive of the appropriate duty cycle to the main horizontal switching transistor Q7, a VMOS power FET. The horizontal oscillator has a startup delay circuit consisting of C12, R27, CR6 and CR7 to allow the power supply to stabilize before drive is applied to Q7. When Q7 is turned on, a current flows into the primary of T1 storing energy as a magnetic field in the core of T1. At the same time, charging current is supplied to capacitor C14 to supply the 40VDC required for the video amplifier and vertical retrace blanking circuits. When Q7 is turned off, energy in the core is supplied through the horizontal width and horizontal linearity controls (L1, C16, and L2) to the deflection yoke. The magnetic field produced by the deflection yoke sweeps the electron beam across the CRT face. Horizontal position is proportional to the amount and polarity of current flowing through the deflection yoke. Capacitors C15 and C16, and linearity coil L1 provide proper wave shaping of the deflection signal. Energy stored in the core of T1 is also supplied to the secondary of T1 providing the voltages necessary for cathode ray tube operation. Diode rectifiers CR9, CR10, CR11, and CR12 develop the DC accelerating and focusing voltages for the CRT. The high voltage at the CRT's anode, for final electron acceleration, is 6kVDC. Display brightness and focus are controlled by R33 and R32 respectively.

3.5.5 Video Control Summary

This section describes the video controls available for adjusting the quality of the CRT display. The video adjustments described in this section are set for the best possible display at the factory just prior to shipping and need be repeated only under extreme circumstances. (Note the following CAUTION.)

WARNING

REMOVAL OF INSTRUMENT COVERS MAY CONSTITUTE AN ELECTRICAL HAZARD AND SHOULD BE ACCOMPLISHED BY QUALIFIED SERVICE PERSONNEL ONLY.

CAUTION

THE BRIGHTNESS CONTROL LOCATED AT THE REAR OF THE INSTRUMENT CAN BE EASILY DISTURBED WHEN WRAPPING THE POWER CORD ON THE REAR FEET. VERIFY THE CORRECT SETTING OF THIS CONTROL BEFORE CONTINUING WITH ADDITIONAL ADJUSTMENTS.

CAUTION

IF THE INSTRUMENT IS PLACED WITHIN A STRONG MAGNETIC FIELD, THE VIDEO DISPLAY MAY BECOME PERMANENTLY OFFSET. IF THIS CONDITION OCCURS, DEGAUSSING THE VIDEOBRIDGE CASE IS REQUIRED TO RETURN THE DISPLAY TO NORMAL OPERATION. THIS MUST BE DONE BEFORE CONTINUING WITH ADDITIONAL ADJUSTMENTS.

Equipment Required:

Flat blade plastic trim tool or "tweaker" (steps 2,3,5,6)

Hex head plastic trim tool (horizontal width, step 4)

Video Adjustments: (See also Table 3-3)

STEP 1. BRIGHTNESS Control - is a knob located on the instrument's rear panel and can be adjusted by hand. Brightness ranges from black (no display) to full brightness.

To make the following adjustments, remove the outer blue cover per instructions given in Section 4.4.2.2 Removal/Replacement Procedure.

The following adjustments are available through the side of the CRT Enclosure Cover. (Refer to Figure 3-21 for trimmer locations.)

WARNING

TO AVOID ELECTRIC SHOCK FROM DANGEROUSLY HIGH VOLTAGES, USE ONLY INSULATED PLASTIC TRIM TOOLS TO PERFORM THE VIDEO ADJUSTMENTS DESCRIBED BELOW.

- STEP 2. FOCUS Control - adjusts the detail of the displayed characters for maximum sharpness. Make adjustment while observing the characters at the center of the CRT display.
- STEP 3. VERTICAL CENTER - adjusts the relationship for the entire display by moving the vertical frame either up or down.
- STEP 4. HORIZONTAL WIDTH (use hex head tool) - adjusts the size of the display by setting the left and right boundaries. The horizontal boundaries for the displayed picture can be compressed or expanded for best display size.

CAUTION

USE OF ANY OTHER TOOL THAN THE RECOMMENDED HEX HEAD PLASTIC TRIM TOOL MAY RESULT IN ELECTRICAL SHOCK OR DAMAGE TO THE TUNING SLUG.

- STEP 5. VERTICAL HEIGHT - adjusts the size of the display by setting the top and bottom boundaries. The vertical boundaries for the displayed picture can be compressed or expanded for best display size.
- STEP 6. CONTRAST Control - adjusts the ratio of the brightness of the displayed characters to the background color.

Table 3-3 is provided as a summary for the video adjustments and includes reference to trimmer locations and sections where additional information is available.

Table 3-3. Summary of Video Controls

ITEM	CONTROL	DESCRIPTION	CIRCUIT DESCRIPTION REFERENCE
①	BRIGHTNESS	Adjusts the brightness of the CRT display	Section 3.5.2 Section 3.5.4
②	FOCUS	Adjusts the detail of the displayed characters on the CRT display	Section 3.5.4
③	VERTICAL CENTER	Moves the vertical frame either up or down	Section 3.5.3
④	HORIZONTAL WIDTH	Adjusts the horizontal size by setting left and right boundaries	Section 3.5.4
⑤	VERTICAL HEIGHT	Adjusts the vertical size by setting top and bottom boundaries	Section 3.5.3
⑥	CONTRAST	Adjusts the ratio of the brightness of the displayed characters to the background color	Section 3.5.1

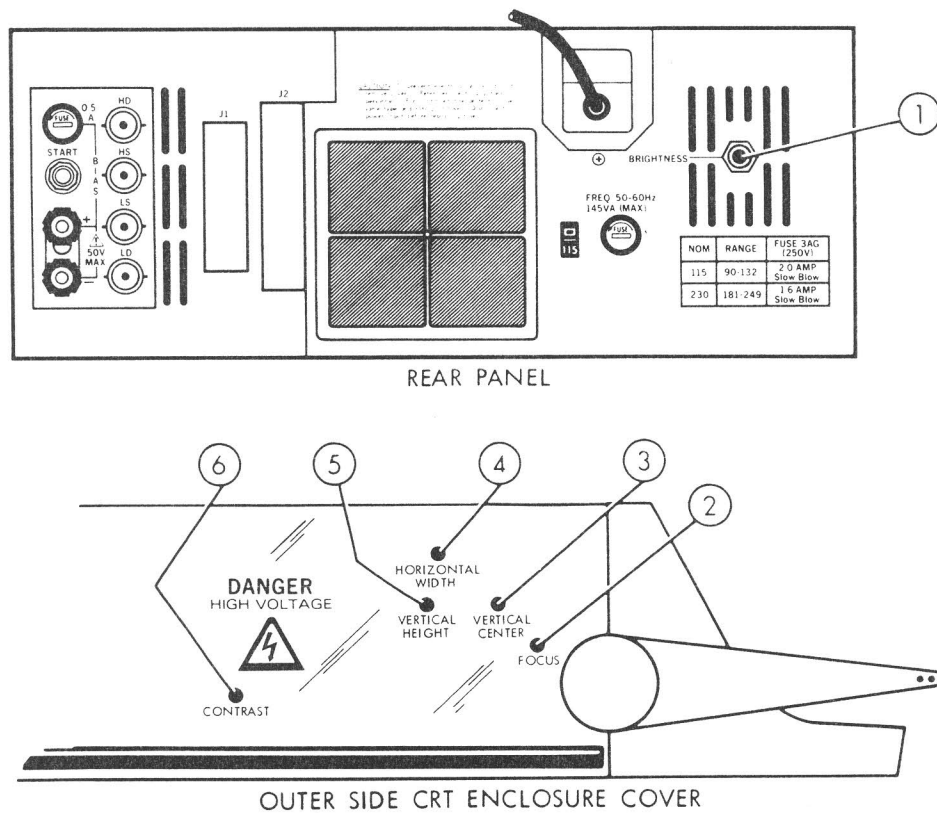


Figure 3-21. Video Control Trimmer Locations

3.6 POWER SUPPLY

WARNING

ALL PARTS OF THE POWER SUPPLY ASSEMBLY INCLUDING INPUT CIRCUIT COMMON ARE AT OR ABOVE POWER LINE VOLTAGE. THE ENERGY AVAILABLE AT ANY POINT ON THE ASSEMBLY MAY BE LIMITED ONLY BY THE INPUT FUSE. DO NOT ATTEMPT SERVICE OPERATIONS. FAILURE TO OBSERVE THIS WARNING MAY RESULT IN SEVERE INJURY OR DEATH.

The Power Supply, under normal conditions, has very dangerous high voltages. Do not attempt to troubleshoot the power supply. If the power supply is suspected of being faulty, send the entire instrument back to ESI for servicing. To determine if a problem exists in the power supply, look at the five LEDs located on the motherboard (see Figure 3-22). Should one or more of these LEDs be dim or dark, the power supply may be faulty and the instrument should be sent to ESI. If all five LEDs are illuminated, the trouble is not in the power supply and normal troubleshooting procedures should be continued.

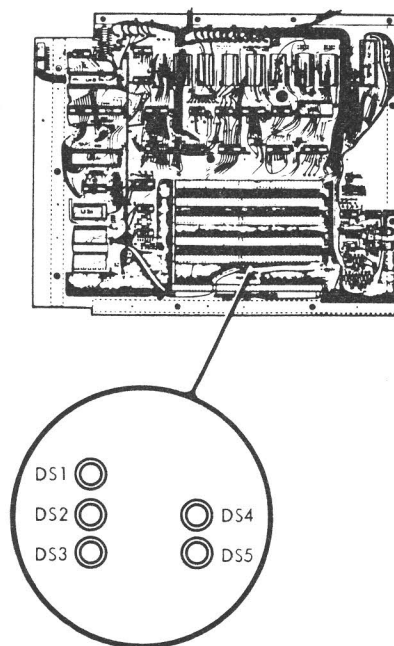


Figure 3-22. Power Supply Diagnostic LED Locations